Efficient perovskite solar cells based on the novel low-temperature processed electron transport layer

With the support by the National Natural Science Foundation of China, the research team led by Prof. Hou Yu (侯宇) and Prof. Yang Huagui (杨化桂) at the Key Laboratory for Ultrafine Materials of Ministry of Education, School of Materials Science and Engineering, East China University of Science and Technology, developed a low-temperature processed In_2S_3 electron transport layer for efficient hybrid perovskite solar cells, which was published in *Nano Energy* (2017, 36: 102—109).

As a new generation of photovoltaics, perovskite solar cells (PSCs) have been intensively studied in recent years due to their high-efficiency, low-cost and ease of fabrication. For a typical high-performance PSC, the electron transport layer (ETL) plays an important role in selectively extracting and transporting photo-generated electrons from perovskite to the electrode. Until now, compact TiO_2 layers are the most widely utilized inorganic ETLs. However, the application of TiO_2 ETL in PSCs is limited due to its high-temperature fabrication and intrinsic slow electron mobility (0.1—1 $cm^2\ V^{-1}\ s^{-1}$).

In this study, for the first time, their group found that a well-organized In_2S_3 nanoflakes array can be used in PSCs with a high power conversion efficiency (PCE) of 18.22% with less hysteresis. In comparison, PSCs based on TiO_2 ETL showed a much lower PCE of 15.70%. Experimental results clearly illustrate that the optimized band structure, enhanced light tapping and low recombination of photo-generated carriers in In_2S_3 ETL-based devices lead to this enhanced performance. Noteworthily, such In_2S_3 ETLs are simple and solution processable at low-temperature (≤80℃), which might provide a new avenue for low-cost and solution-processed photovoltaics.

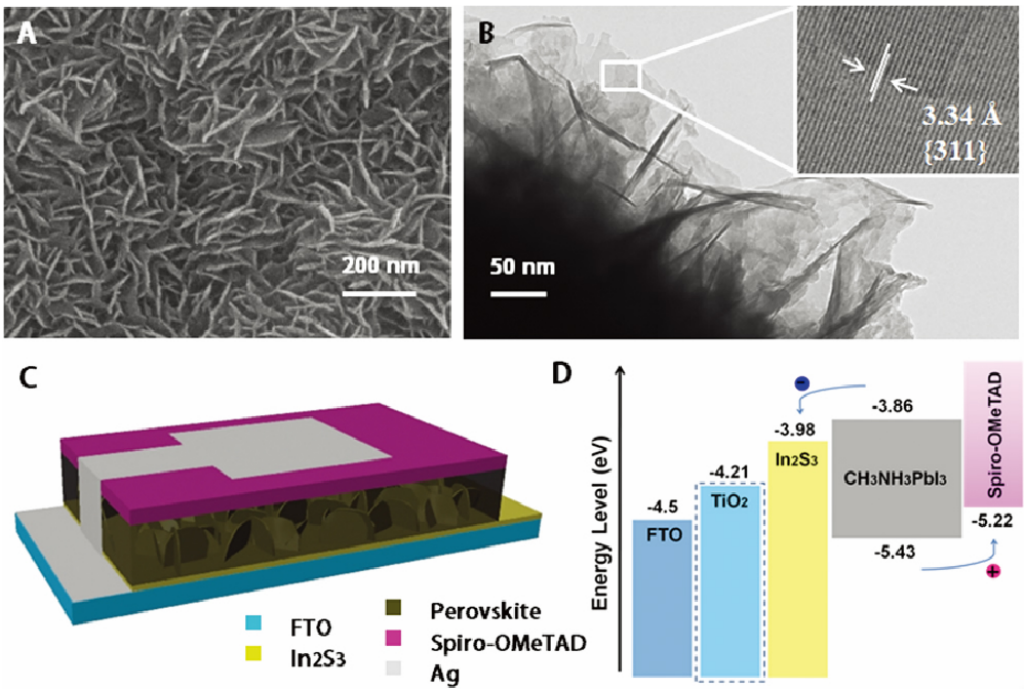

Figure SEM image (A) and high-resolution TEM image (B) of the In_2S_3 nanoflake array, where the inset shows the lattice fringes with interplanar spacing; (C) device architecture of a typical PSC device; (D) schematic diagram of the PSC, showing the separation and transport of photogenerated electrons and holes.